IN THE CLAIMS

Please cancel without prejudice claims 2-3, 5, 12-13, 15, 24, and 26.

Please amend claims 1, 4, 6, 11, 14, 16, 21, 25, 27-28, 30-32, 37-39, and 44.

1.   (Currently Amended) An apparatus, comprising:

a first register to store default configuration data;

a second register coupled to the first register to store active configuration data;

an input circuit coupled to the second register to receive input data different than the

default configuration data to be programmed into the second register; and

control logic coupled to the first register, the second register, and the input circuit to

load the second register with data selected from either the default configuration

data from the first register or input data from the input circuit; and

reset logic coupled to the first register and the second register to select between

loading the second register with the default configuration data and retaining a

previous content of the second register in the second register, the rest logic

including

a first reset line to carry a first reset signal to load default data from the first

register into the second register,

a second reset line coupled to the programmable selection circuit to carry a

second reset signal, and

a programmable selection circuit to store a selection value to determine if the

second reset signal causes the second register to be loaded with the

default configuration data from the first register or causes the second

register to retain its data

2. – 3.   (Canceled)

4.   (Currently Amended) The apparatus of claim [[3]] 1,wherein the first reset line is a
power-up reset line.

5.   (Canceled)

6.   (Currently Amended) The apparatus of claim [[5]] 1, wherein the second reset line is
a warm-start reset line.

7.   (Original) The apparatus of claim 1, wherein the input circuit is to receive write data
          from a data bus, the write data comprising programmable configuration data.

8.   (Original) The apparatus of claim 1, wherein the first register is a non-volatile
register.

9.   (Original) The apparatus of claim 1, wherein the second register is a volatile register.

10.   (Original) The apparatus of claim 1, wherein the default configuration data defines a
first memory configuration and the programmable configuration data defines a second
memory configuration.

11.   (Currently Amended) A system, comprising:

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a processor;

a memory subsystem coupled to the processor and comprising flash memory, the

memory subsystem including:

a first register to store default configuration data;

a second register coupled to the first register to store active configuration data;

an input circuit coupled to the second register to receive input data different

than the default configuration data to be programmed into the second

register; and

control logic coupled to the first register, the second register, and the input

circuit to load the second register with data selected between the default

configuration data from the first register and input data from the input

circuit; and

reset logic coupled to the first register and the second register to select between

loading the second register with the default configuration data and

retaining a previous content of the second register in the second

register, the rest logic including

a first reset line to carry a first reset signal to load default data from the

first register into the second register,

a second reset line coupled to the programmable selection circuit to

carry a second reset signal, and

a programmable selection circuit to store a selection value to determine

if the second reset signal causes the second register to be loaded

with the default configuration data from the first register or

causes the second register to retain its data.

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12. – 13.   (Canceled)

14.   (Currently Amended) The system of claim [[13]] 11,wherein the first reset line is a
power-up reset line.

15.   (Canceled)

16.   (Currently Amended) The system of claim [[15]] 11, wherein the second reset line is a
warm-start reset line.

17.   (Original) The system of claim 11, wherein the input circuit is to receive write data
from a data bus, the write data comprising programmable configuration data.

18.   (Original) The system of claim 11, wherein the first register is a non-volatile register.

19.   (Original) The system of claim 11, wherein the second register is a volatile register.

20.   (Original) The system of claim 11, wherein the default configuration data defines a
first memory configuration and the programmable configuration data defines a second
memory configuration.

21.   (Currently Amended) A method, comprising:
         providing, in a memory device, a first register containing default configuration data;

selecting active configuration data from between the default configuration data in the

first register and input data from an input logic circuit, the input logic circuit

receiving the input data different than the default configuration data;

writing the active configuration data into a second register; ~~and~~

loading the default configuration data from the first register into the second register

upon assertion of a first reset signal;

selecting, upon assertion of a second reset signal, between retaining the active

configuration data in the second register and loading the default configuration

data from the first register into the second register; and

using the active configuration data in the second register to specify a configuration.

22.   (Original) The method of claim 21, wherein providing the first register includes

providing a non-volatile register.

23.   (Original) The method of claim 21, wherein writing into the second register includes

writing into a volatile register.

24.   (Canceled) .

25.   (Currently Amended) The method of claim [[24]] 21, wherein assertion of a first reset

signal includes assertion of a power-up reset signal.

26.   (Canceled)

27.   (Currently Amended) The method of claim [[26]] 21, wherein assertion of a second

reset signal includes assertion of a warm-start reset signal.

28.   (Currently Amended) The method of claim [[26]] 21, wherein selecting active

configuration data includes selecting programmable configuration data from the input

logic circuit to define an operational configuration of a memory that is different than

defined by the default configuration data.

29.   (Original) The method of claim 21, wherein selecting active configuration data

includes selecting default configuration data to define a predetermined intended operational

configuration of a memory.

30.   (Currently Amended) The apparatus of claim [[3]] 1, wherein the input data is

programmed into the second register when a write-enable signal is asserted at an enable input

of the second register and when the first reset line is de-asserted.

31.   (Currently Amended) The apparatus of claim [[5]] 1, wherein the second register is

programmed with the default configuration data when the second reset line is asserted and the

value of the programmable selection circuit has a logical value of one, and wherein the second

register is to the retain previous content when the second reset line is asserted and the value of

the programmable selection circuit has a logical value of zero.

32.   (Currently Amended) The apparatus of claim [[5]] 1, further comprising a first OR

gate, wherein the second reset line is coupled to a non-inverted input of the first OR gate and

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the programmable selection circuit is coupled to an inverted input of the first OR gate, and

wherein an output of the first OR gate is used to determine whether the second register is

programmed with the default configuration data or the second register is to retain the previous

content.

33.   (Previously Presented)   The apparatus of claim 32, further comprising an AND

gate, wherein the first reset line is coupled to a first input of the AND gate and the output of

the first OR gate is coupled to a second input of the AND gate, and wherein an output of the

AND gate is used to determine whether the second register is programmed with the default

configuration data or the second register is to retain the previous content.

34.   (Previously Presented)   The apparatus of claim 33, further comprising:

    a second OR gate coupled to the first register and having an output coupled to a set

        input of the second register; and

    a third OR gate coupled to the first register and having an output coupled to a reset

        input of the second register, the second OR gate setting the second register to a

        logical value of one and the third OR gate resetting the second register to a

        logical value of zero.

35.   (Previously Presented)   The apparatus of claim 34, wherein the second OR gate

comprises an inverted input to receive an output from the first register and a non-inverted

input to receive an output from the AND gate.

36.   (Previously Presented)   The apparatus of claim 34, wherein the third OR gate

comprises a first input to receive an output from the first register and a second input to receive

an output from the AND gate.

37.   (Currently Amended) The system of claim [[13]] 11, wherein the input data is

programmed into the second register when a write-enable signal is asserted at an enable input

of the second register and when the first reset line is de-asserted.

38.   (Currently Amended) The system of claim [[15]] 11, wherein the second register is

programmed with the default configuration data when the second reset line is asserted and the

value of the programmable selection circuit has a logical value of one, and wherein the second

register is to the retain previous content when the second reset line is asserted and the value of

the programmable selection circuit has a logical value of zero.

39.   (Currently Amended) The system of claim [[15]] 11, wherein the memory subsystem

further comprises a first OR gate, wherein the second reset line is coupled to a non-inverted

input of the first OR gate and the programmable selection circuit is coupled to an inverted

input of the first OR gate, and wherein an output of the first OR gate is used to determine

whether the second register is programmed with the default configuration data or the second

register is to retain the previous content.

40.   (Previously Presented)   The system of claim 39, wherein the memory subsystem

further comprises an AND gate, wherein the first reset line is coupled to a first input of the

AND gate and the output of the first OR gate is coupled to a second input of the AND gate,

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and wherein an output of the AND gate is used to determine whether the second register is programmed with the default configuration data or the second register is to retain the previous content.

41.   (Previously Presented)   The system of claim 40, wherein the memory subsystem further comprises:

    a second OR gate coupled to the first register and having an output coupled to a set
        input of the second register; and
    a third OR gate coupled to the first register and having an output coupled to a reset
        input of the second register, the second OR gate setting the second register to a
        logical value of one and the third OR gate resetting the second register to a
        logical value of zero.

42.   (Previously Presented)   The system of claim 41, wherein the second OR gate comprises an inverted input to receive an output from the first register and a non-inverted input to receive an output from the AND gate.

43.   (Previously Presented)   The system of claim 41, wherein the third OR gate comprises a first input to receive an output from the first register and a second input to receive an output from the AND gate.

44.   (Currently Amended) The method of claim [[24]] 21, wherein the input data is programmed into the second register when a write-enable signal is asserted at an enable input of the second register and when the first reset signal is de-asserted.

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45.   (Previously Presented)   The method of claim 28, wherein the second register is

programmed with the default configuration data when the second reset signal is asserted and

the value of the programmable selection circuit has a logical value of one, and wherein the

second register is to the retain previous content when the second reset signal is asserted and

the value of the programmable selection circuit has a logical value of zero.

46.   (Previously Presented)   The method of claim 28, further comprising:

coupling the second reset signal to a non-inverted input of a first OR gate;

coupling the programmable selection circuit to an inverted input of the first OR gate;

    and

determining whether the second register is programmed with the default configuration

        data or the second register is to retain the previous content, based on an output

        of the first OR gate.

47.   (Previously Presented)   The method of claim 46, further comprising:

coupling the first reset signal to a first input of an AND gate;

coupling the output of the first OR gate to a second input of the AND gate; and

determining whether the second register is programmed with the default configuration

        data or the second register is to retain the previous content, based on an output

        of the AND gate.

  48.   (Previously Presented)   The method of claim 47, further comprising:

coupling a second OR gate to the first register and having an output coupled to a set

    input of the second register; and

coupling a third OR gate to the first register and having an output coupled to a reset

    input of the second register, the second OR gate setting the second register to a

    logical value of one and the third OR gate resetting the second register to a

    logical value of zero.

49.   (Previously Presented)   The method of claim 48, wherein the second OR gate

comprises an inverted input to receive an output from the first register and a non-inverted

input to receive an output from the AND gate.

50.   (Previously Presented)   The method of claim 48, wherein the third OR gate

comprises a first input to receive an output from the first register and a second input to receive

an output from the AND gate.